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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 10/627,648 | 07/28/2003 | Koji Usuda | 04329.3101 | 3609 |

7590 11/16/2004
Finnegan, Henderson, Farabow,
Garrett & Dunner, L.L.P.
1300 I Street, N.W.
Washington, DC 20005-3315

EXAMINER

CAO, PHAT X

| ART UNIT | PAPER NUMBER |
|----------|--------------|
|----------|--------------|

2814

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary

Application No.

10/627,648

Applicant(s)

USUDA ET AL.

Examiner

Phat X. Cao

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>7/03&8/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.
2. The cancellation of claims 13-19 in paper filed 8/9/04 is acknowledged.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 4-7 and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imai et al (US. 5,847,419) in view of Nishikawa et al (Advanced LSI Technology Laboratory, Toshiba Corporation, pp. 174-175 – cited by applicant).

Regarding claims 1, 4-5, 7, and 10-11, Imai (Fig. 3K) discloses a semiconductor apparatus comprising: a substrate 11; a buffer layer 15 made of monocrystal SiGe (column 10, lines 8-16) and formed on the substrate 11; a strained-silicon layer 16 (column 8, lines 42-45) formed on the buffer layer 15; a source region 22b and a drain region 22a formed in the strained-silicon layer 16 so as to be separated from each other; a gate insulating film 20 formed on the strained-silicon layer 16 sandwiched between the source/drain regions; and a gate electrode 21 formed on the gate insulating film 20. It is noted that because the silicon layer 16 is strained (column 8, lines 42-45), the underlay buffer layer 15 would have lattice constant which is different from that of the silicon layer 16.

Imai does not disclose the gate insulating film 20 made of a monocrystal rare earth oxide having a lattice constant different from that of silicon 16.

However, Nishikawa teaches the forming of a gate insulating film on the silicon layer, and made of a monocrystal rare earth oxide of CeO₂ having a lattice constant different from that of silicon (i.e., $d=0.35\%$) (see Introduction on page 174). Accordingly, it would have been obvious to use the monocrystal rare earth oxide of CeO₂ as an alternative dielectric for the gate oxide 20 of Imai because as taught by Nishikawa, such single crystalline CeO₂ would provide an ultra-thin gate dielectric having high-K dielectric constant (see page 174).

Regarding claims 6 and 12, Imai's Fig. 3K further discloses that the buffer layer 15 is formed on the silicon substrate 11 through the insulating film 14.

5. Claims 2-3 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imai et al and Nishikawa as applied to claim (1, 7) above, and further in view of Hisamoto et al (US. 2003/0137017).

Neither Imai nor Nishikawa discloses the gate electrode made of crystalline SiGe.

However, Hisamoto (Fig. 1) teaches the forming of a gate electrode 11 made of crystalline SiGe (par. [0040]). Accordingly, it would have been obvious to use the crystalline SiGe as an alternative material for the gate electrode because as taught by Hisamoto, such crystalline SiGe gate electrode would provide a different work function depending on its composition ratio (par. [0041]).


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6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
November 12, 2004


PHAT X. CAO
PRIMARY EXAMINER